

TITLE OF THE INVENTION

NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF  
MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

5           This application is based upon and claims the  
benefit of priority from the prior Japanese Patent  
Application No. 2002-199915, filed July 9, 2002, the  
entire contents of which are incorporated herein by  
reference.

10                           BACKGROUND OF THE INVENTION

1. Field of the Invention

          The present invention relates to a non-volatile  
semiconductor memory device and a method of manufactur-  
ing the same. More particularly, the present invention  
15       relates to a NAND-type flash memory, which includes  
a floating gate electrode and two or more gate oxide  
films having a different thickness in peripheral and  
cell sections.

2. Description of the Related Art

20       Recently, the development of a NAND-type flash  
memory has been made. The NAND-type flash memory is  
formed by gate pre-forming (or gate oxide film pre-  
forming) process. According to the gate pre-forming  
process, trench isolation is employed, and several gate  
25       oxide films having different thickness are separately  
formed.

          However, in the NAND-type flash memory, gate oxide

films 101a and 102a on a silicon (Si) substrate 103 are different in their thickness between a cell/Vcc section 101 and a Vpp section 102, as shown in FIG. 5A.

For this reason, a step (a) is formed in the upper

5 surface of SiN films (stopper SiN films) 101c and 102c on gate electrodes 101b and 102b. For example, the step (a) is a factor of causing the following disadvantage in shallow-trench isolation (STI)

formation. As illustrated in FIG. 5B, a difference

10 is made in the thickness of SiN films when the upper surface of a buried insulator 104 is removed by chemical mechanical polishing (CMP) using SiN films 101c and 102c as a stopper. More specifically, the SiN film 102c of the Vpp section 102 is thinner than the

15 SiN film 101c of the cell/Vcc section 101. The excess thickness reduction of the SiN film 102c is a factor of reducing the a height (h) to the gate oxide film 102a.

As a result, the gate oxide film 102a is easily damaged by etching (e.g., wet etching) after CMP. The gate

20 oxide film 102a being damaged is a factor in causing failure such as gate leakage.

In particular, the NAND-type flash memory has a high-voltage row decoder circuit 111. As shown in FIG. 6, the row decoder circuit 111 is arranged in

25 a peripheral region (corresponding to Vpp section 102) adjacent to a cell array region (Cell Array) 110 corresponding to the cell/Vcc section 101. Normally,

the row decoder circuit 111 is formed using a gate oxide film for Vpp system (Vpp oxide film 102a). In other words, a high-voltage transistor exists in the row decoder circuit 111 of the NAND-type flash memory.

5           Conversely, a Vcc oxide film 101a is used, in general, in the cell array region 110, a guard ring 112 arranged between the cell array region 110 and the row decoder circuit 111 and a dummy AA pattern 113 near the row decoder circuit 111. For this reason, when a film  
10           to make a buried insulator 104 is subjected to CMP in STI formation, the SiN film 102c of the row decoder circuit 111 is excessively reduced in thickness as compared with the SiN film 101c. This is a factor in causing the foregoing failure.

15           In the conventional case, it is possible to readily realize the NAND-type flash memory having several gate oxide films of different thicknesses according to the gate pre-forming process. However, the stopper SiN film of the row decoder circuit is  
20           greatly reduced in thickness by CMP in the STI formation. As a result, the gate oxide film under the stopper SiN film is easily damaged; for this reason, there is a problem that failure such as gate leakage occurs.

25                           BRIEF SUMMARY OF THE INVENTION

          According to a first aspect of the present invention, there is provided a non-volatile

semiconductor memory device comprising: a semiconductor substrate; a memory cell array formed on the semiconductor substrate, and including a first gate insulator having a first thickness; a high-voltage transistor circuit formed on the semiconductor substrate, and including a second gate insulator having a second thickness greater than the first thickness; and a peripheral circuit formed on the semiconductor substrate, and including the second gate insulator.

According to a second aspect of the present invention, there is provided a method of manufacturing a non-volatile semiconductor memory device, comprising: successively depositing a first gate insulator having a first thickness, a first gate electrode film and a first mask insulator on a semiconductor substrate; leaving the first gate insulator, the first gate electrode film and the first mask insulator in only array region; separately forming the following gate insulators in a peripheral region excepting the array region, that is, forming a second gate insulator having a second thickness greater than the first thickness in a first region of a peripheral region, and forming a third gate insulator having a thickness the same as the first thickness in a second region of the peripheral region; successively depositing a second gate electrode film and a second mask insulator thicker than the first mask insulator on each of the first mask insulator,

the second gate insulator and the third gate insulator;  
removing the second mask insulator and the second gate  
electrode film on the first mask insulator; forming  
an isolation trench on a surface of the semiconductor  
substrate to correspond to each position between the  
5 array region and first and second regions of the  
peripheral region; depositing a buried insulator on  
the entire surface; and polishing an upper surface of  
the buried insulator so that the upper surface can be  
10 planarized.

According to a third aspect of the present  
invention, there is provided a method of manufacturing  
a non-volatile semiconductor memory device, comprising:  
successively depositing a first gate insulator having  
15 a first thickness, a first gate electrode film and  
a first mask insulator on a semiconductor substrate;  
leaving the first gate insulator, the first gate  
electrode film and the first mask insulator in only an  
array region and a first peripheral region; forming a  
20 second gate insulator having a second thickness greater  
than the first thickness in a second peripheral region  
excepting the array region and the first peripheral  
region; successively depositing a second gate electrode  
film thinner than the first gate electrode film and  
25 a second mask insulator on each of the first mask  
insulator and the second gate insulator; removing the  
second mask insulator and the second gate electrode

film on the first mask insulator; forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and first and second regions of the peripheral region; depositing a buried insulator on the entire surface; and polishing an upper surface of the buried insulator so that the upper surface can be planarized.

According to a fourth aspect of the present invention, there is provided a method of manufacturing a non-volatile semiconductor memory device, comprising: previously forming a recess in a first peripheral region on a semiconductor substrate; forming a first gate insulator having a first thickness in the recess; forming a second gate insulator having a second thickness less than the first thickness in an array region and a second peripheral region on the semiconductor substrate; successively depositing first and second gate electrode films and first and second mask insulators on each of the first and second gate insulators; forming an isolation trench on a surface of the semiconductor substrate to correspond to each position between the array region and the first and second regions of the peripheral region; depositing a buried insulator on the entire surface; and polishing an upper surface of the buried insulator so that the upper surface can be planarized.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1A is a plan view showing a NAND-type flash memory according to a first embodiment of the present invention, and FIG. 1B is a cross-sectional view taken  
5 along a line IB-IB of FIG. 1A;

FIG. 2A to FIG. 2D are process cross-sectional views to explain a method of manufacturing a NAND-type flash memory according to a second embodiment of the present invention;

10 FIG. 3A to FIG. 3D are process cross-sectional views to explain a method of manufacturing a NAND-type flash memory according to a third embodiment of the present invention;

15 FIG. 4A to FIG. 4C are process cross-sectional views to explain a method of manufacturing a NAND-type flash memory according to a fourth embodiment of the present invention;

FIG. 5A and FIG. 5B are cross-sectional views showing the process of manufacturing a NAND-type flash memory to explain the prior art and the problem; and  
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FIG. 6 is a plan view showing a conventional a NAND-type flash memory.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention will be  
25 described below with reference to the accompanying drawings.

(First embodiment)

FIG. 1A and FIG. 1B show the structure of a NAND-type flash memory formed by gate pre-forming (or gate oxide pre-forming) process according to a first embodiment of the present invention. FIG. 1A is a plan view showing principal parts of the NAND-type flash memory, and FIG. 1B is an enlarged view showing the sectional structure substantially corresponding to line IB-IB of FIG. 1A.

In the NAND-type flash memory, a cell array 21 is formed in an array region on a Si substrate 11. A high-voltage row decoder circuit (high-voltage transistor) 31 is formed in a peripheral region adjacent to the cell array 21. A guard ring 41 functioning as a peripheral circuit is formed between the cell array 21 and the row decoder circuit 31. The peripheral region is formed with a dummy AA pattern (peripheral circuit) near the row decoder circuit 31.

In the cell array 21, an N-well region (Cell N-well) 21A is formed on the surface of the Si substrate 11. In the N-well region 21A, a P-well region (Cell P-well) 21B is formed. A plurality of memory cells (not shown) are formed on the surface of the P-well region 21B. Each memory cell has a structure in which a poly gate electrode (first gate electrode film) 21b and a SiN film (first mask insulator) 21c are stacked on a Vcc gate oxide film



(Vcc oxide film) 21a. The poly gate electrode includes such as poly silicon, polycide and the like. The gate oxide film 21a is a first gate insulator having a first thickness. The SiN film 12c functions as the stopper in CMP.

Conversely, the row decoder circuit 31, guard ring 41 and dummy AA pattern 51 are formed using high breakdown voltage (Vpp) gate oxide films (Vpp oxide film) 31a, 41a and 51a, respectively. Each of the gate oxide films 31a, 41a and 51a is a second gate insulator having a second thickness greater than the first thickness of the gate oxide film 21a. In other words, the row decoder circuit 31 includes a high-voltage transistor (not shown) formed on the surface of the Si substrate 11. The high-voltage transistor has a structure in which a poly gate electrode (second gate electrode film) 31b and a SiN film (second mask insulator) 31c are stacked on the Vpp gate oxide film 31a. The SiN film 31c functions as the stopper in CMP. The guard ring 41 is formed on each surface of well regions 21A, 21B and N-well (NW) 41A. Each guard ring 41 has a structure in which a poly gate electrode (second gate electrode film) 41b and a SiN film (second mask insulator) 41c are stacked on the Vpp gate oxide film 41a. The SiN film 41c functions as the stopper in CMP. The dummy AA pattern 51 is formed on the surface of the Si substrate 11 adjacent to the row decoder

circuit 31. The dummy AA pattern 51 has a structure in which a poly gate electrode (second gate electrode film) 51b and a SiN film (second mask insulator film) 51c are stacked on the Vpp gate oxide film 51a.

5 The SiN film 51c functions as the stopper in CMP.

An STI isolation region 12 burying insulator is formed between regions (21 and 41, 41 and 31, 31 and 51).

Conventionally, the guard ring and dummy pattern  
10 in the periphery of the row decoder circuit have been formed using a Vcc oxide film. The guard ring and dummy pattern are formed in a high-breakdown-voltage oxide film region. Namely, the guard ring 41 and the dummy AA pattern 51 are formed using Vpp oxide films  
15 41a and 51a, respectively. In this way, it is possible to offset the step (global step shown by "a" in FIG. 5A) on the upper surface of the stopper SiN film 31c around the high-voltage transistor of the row decoder circuit 31. As a result, the SiN film 31 is  
20 prevented from being excessively reduced in thickness, so that a sufficient height (h) to the Vpp oxide film 31a can be secured.

The structure described above is employed, and thereby, the following effect is obtained. It is  
25 possible to prevent only residual film thickness of the SiN film 31c from being greatly reduced between the guard ring 41 and the row decoder circuit 31 and

between the row decoder circuit 31 and the dummy AA pattern 51. Therefore, it is possible to solve the conventional problem of reducing a margin for CMP when gate pre-forming process is employed because the NAND-type flash memory has the high-voltage transistor in the row decoder section. As a result, the Vpp oxide film 31a of the row decoder circuit 31 is prevented from being easily damaged, and failure such as gate leakage is prevented.

(Second embodiment)

FIG. 2A to FIG. 2D show a method of manufacturing a NAND-type flash memory formed by gate pre-forming process according to a second embodiment of the present invention. Here, the cell section formed with the cell array has a different structure with the Vcc section formed with a guard ring and a dummy AA pattern.

As shown in FIG. 2A, the following films are formed in the array region (cell section) on the Si substrate 11. The films are Vcc oxide film (first gate insulator 21a having the first thickness, poly gate electrode (first gate electrode film) 21b and stopper SiN film (first mask insulator) 21c. In this case, various materials are deposited on the Si substrate 11, and thereafter, patterning is carried out. The Vcc oxide film 21a, poly gate electrode 21b and stopper SiN film 21c formed in peripheral regions (Vpp section/Vcc section) other than the array region are removed.

In this way, the Si substrate 11 of the peripheral region is exposed.

As illustrated in FIG. 2B, one region (Vpp section) of the peripheral regions on the Si substrate is formed with the Vpp oxide film (second gate insulator) 31a having a second thickness greater than the first thickness of the Vcc oxide film 21a. The other region (Vcc section) of the peripheral regions is formed with Vcc oxide films (third gate insulator) 41a' and 51a' having a thickness the same as the first thickness of the Vcc oxide film 21a. Thereafter, a poly gate electrode material 61b and stopper SiN film material 61c are successively deposited on the stopper SiN film 21c, Vpp oxide film 31a and Vcc oxide films 41a' and 51a'. In this case, the thickness of the stopper SiN film material 61c is made greater than that of the stopper SiN film 21c.

As depicted in FIG. 2C, the poly gate electrode material 61b and stopper SiN film material 61c formed on the cell section is removed. In this way, the poly gate electrode (second gate electrode film) 31b and the stopper SiN film (second mask insulator) 31c are stacked on the Vpp oxide film 31a of the Vpp section. The poly gate electrodes (second gate electrode film) 41b, 51b and the stopper SiN film (second mask insulator) 41c, 51c are stacked on the Vcc oxide film 41a' and 51a' of the Vcc section, respectively.

As seen from FIG. 2D, an isolation trench 71 is correspondingly formed on the surface of the Si substrate 11 between the cell section and peripheral regions, that is, Vpp section/Vcc section (STI formation). A buried insulator 72 is deposited, and thereafter, planarizing by CMP is carried out, and thus, a STI-structure isolation 12 is formed.

Thereafter, memory cell, row decoder circuit (high-voltage transistor), and guard ring and dummy AA pattern are formed with respect to cell section, Vpp section, and Vcc section, respectively (although these formations are not shown). In this manner, a NAND-type flash memory is realized.

In the embodiment, the SiN film material 61c (31c, 41c, 51c) of the peripheral regions (i.e., Vcc and Vpp sections) is formed to be thicker than the SiN film material 21c of the cell section. In this way, it is possible to prevent the thickness of the SiN film 31c from being reduced by CMP. In addition, it is possible to make large enough the height h1 to the Vpp oxide film 31a and the height h2 to Vcc oxide film 41a', 51a'. Therefore, this serves to prevent gate oxide film (Vpp oxide film 31a) from being damaged in the process after CMP; as a result, a sufficient margin for CMP can be achieved.

As described above, the SiN film used as the stopper in CMP for STI formation is formed separately

in its thickness in the cell section and the peripheral regions. More specifically, the SiN film of the Vpp section is formed to be thicker than that of the cell section. In this way, it is possible to increase  
5 the residual film thickness of the SiN film of the high-voltage transistor in process. As a result, a sufficient margin for CMP can be achieved.

In addition, the second embodiment has the following advantage, unlike the first embodiment.  
10 Namely, Vcc oxide films 41a' and 51a' of the guard ring 41 and the dummy AA pattern 51 formed in the Vcc section need not be formed to have the same thickness as the Vpp oxide film 31a.

(Third embodiment)

15 FIG. 3A to FIG. 3D show a method of manufacturing a NAND-type flash memory formed by gate pre-forming process according to a third embodiment of the present invention. Here, the cell section formed with the cell array and the Vcc section formed with the guard ring  
20 and the dummy AA pattern have the same structure.

As shown in FIG. 3A, the following films are formed in the array region (cell section) and Vcc section (first peripheral region) on the Si substrate 11. The films are Vcc oxide films (first gate  
25 insulator) 21a, 41a' and 51a' having the first thickness, poly gate electrodes (first gate electrode film) 21b, 41b and 51b and stopper SiN films (first

mask insulator) 21c, 41c and 51c. In this case, various materials are deposited on the Si substrate 11, and thereafter, patterning is carried out. The Vcc oxide films 21a, 41a' 51a', poly gate electrodes 21b, 41b, 51b and stopper SiN films 21c, 41c, 51c formed in a Vpp section (second peripheral region) other than the array region and the Vcc section are removed. In this way, the Si substrate 11 of the Vpp section is exposed.

As illustrated in FIG. 3B, the Vpp section on the Si substrate is formed with the Vpp oxide film (second gate insulator) 31a having the second thickness thicker than the Vcc oxide film 21a. Thereafter, a poly gate electrode material 61b and stopper SiN film material 61c are successively deposited on the stopper SiN films 21c, 41c, 51c and the Vpp oxide film 31a. In this case, the thickness of the poly gate electrode material 61b is made thinner than the poly gate electrodes 21b, 41b and 51b. In addition, the stopper SiN film material 61c is deposited to be flush with the upper surface of the stopper SiN films 21c, 41c and 51c.

As depicted in FIG. 3C, the poly gate electrode material 61b and stopper SiN film material 61c formed on the cell and Vcc sections are removed. In this way, the poly gate electrode (second gate electrode film) 31b and the stopper SiN film (second mask insulator) 31c are stacked on the Vpp oxide film 31a of the Vpp section.

As seen from FIG. 3D, an isolation trench 71 is correspondingly formed on the surface of the Si substrate 11 between the cell section and the Vpp/Vcc section (STI formation). A buried insulator 72 is deposited, and thereafter, planarizing by CMP is carried out, and thus, a STI isolation 12 is formed.

Thereafter, memory cell, row decoder circuit (high-voltage transistor) and guard ring and dummy AA pattern are formed with respect to cell section, Vpp section and Vcc section, respectively (these formations are not shown). In this way, a NAND-type flash memory is realized.

In the embodiment, stopper SiN films 31c and 21c of the row decoder circuit and the cell section are readily formed in a state their upper surfaces are flush with each other. In this way, it is possible to prevent an extra reduction of the thickness of the SiN film 31c in CMP, and to sufficiently take the height to the Vpp oxide film 31a. Therefore, this serves to prevent the gate oxide film (Vpp oxide film 31a) from being damaged in the process after CMP; as a result, a sufficient margin for CMP can be achieved.

As described above, the SiN film used as the stopper in CMP for STI formation is formed separately in its thickness in the cell section and the Vpp section. More specifically, stopper SiN films of the Vpp section and the cell section are readily formed



in the state that their upper surfaces are flush with each other. In this way, it is possible to increase the residual film thickness of the SiN film of the high-voltage transistor in process. As a result,  
5 a sufficient margin for CMP can be achieved.

In addition, according to the third embodiment, only Vpp oxide film 31a can be formed to be thicker than Vcc oxide films 41a' and 51a', like the second embodiment described before.

10 (Fourth embodiment)

FIG. 4A to FIG. 4C show a method of manufacturing a NAND-type flash memory formed by gate pre-forming process according to a fourth embodiment of the present invention. Here, the cell section formed with the cell  
15 array and the Vcc section formed with guard ring and dummy AA pattern have the same structure.

As shown in FIG. 4A, the surface of the Si substrate 11 is selectively etched using a photo engraving process (PEP) and dry etching techniques.  
20 In this way, the Vpp section (first peripheral region) is formed with a recess 81, which has a height lower than the cell and Vcc sections. In this case, the depth of the recess 81 is approximately the same as the thickness of the Vpp oxide film (first gate  
25 insulator) formed therein.

As illustrated in FIG. 4B, a Vpp oxide film 31a having a first thickness is formed in the recess 81

formed at the Vpp section on the Si substrate 11. Vcc oxide films (second gate insulator) 21a, 41a' and 51a' having a second thickness less than that of the Vpp oxide film 31a are formed in the array region (cell section) and the Vcc section (second peripheral region) on the Si substrate 11. Thereafter, a poly gate electrode material 61b and stopper SiN film material 61c are successively deposited on the Vcc oxide films 21a, 41a, 51a and the Vpp oxide film 31a. In this way, poly gate electrodes (second gate electrode film) 21b, 41b, 51b and stopper SiN films (second mask insulator) 21c, 41c, 51c are stacked on the Vcc oxide films 21a, 41a' and 51a' of the cell and Vcc sections. The poly gate electrode (first gate electrode film) 31b and the stopper SiN film (first mask insulator) 31c are stacked on the Vpp oxide film 31a of the Vpp section. In this case, the Vpp oxide film 31a is formed in the recess 81, and thereby, the surface of the stopper SiN film 31c is approximately flush with that of the stopper SiN films 21c, 41c and 51c.

As depicted in FIG. 4C, an isolation trench 71 is correspondingly formed on the surface of the Si substrate 11 between the cell/Vcc section and the Vpp section, that is, Vpp section/Vcc section (STI formation). A buried insulator 72 is deposited, and thereafter, planarizing by CMP is carried out, and thus, a STI isolation 12 is formed.

Thereafter, a memory cell, row decoder circuit (high-voltage circuit) and guard ring and dummy AA pattern are formed with respect to the cell section, Vpp section and Vcc section, respectively (these  
5 formations are not shown). In this way, a NAND-type flash memory is realized.

In the embodiment, the silicon surface of the Vpp section is positioned lower than the cell section by the film thickness of the Vpp oxide film 31a. Thus,  
10 the upper surface of the SiN film 31c is readily flush with that of the SiN film 21c of the cell section. In this way, it is possible to prevent an excess reduction of thickness of the SiN film 31c by CMP, and to achieve a sufficient height to the Vpp oxide film  
15 31a. Therefore, this serves to prevent gate oxide film (Vpp oxide film 31a) from receiving damage in process after CMP; as a result, a sufficient margin for CMP can be achieved.

As described above, the SiN film used as the  
20 stopper in CMP for STI formation is formed separately in its thickness in the cell section and peripheral regions. More specifically, the stopper SiN film of the Vpp section is formed to have the same thickness as that of the cell section. In this way, it is  
25 possible to increase the residual film thickness of the SiN film of the high-voltage transistor in process. As a result, the margin for CMP can be sufficiently

obtained.

In addition, according to the fourth embodiment,  
only Vpp oxide film 31a can be formed to be thicker  
than Vcc oxide films 41a' and 51a', like the second and  
5 third embodiment described before.

Additional advantages and modifications will  
readily occur to those skilled in the art. Therefore,  
the invention in its broader aspects is not limited to  
the specific details and representative embodiments  
10 shown and described herein. Accordingly, various  
modifications may be made without departing from the  
spirit or scope of the general inventive concept as  
defined by the appended claims and their equivalents.